The Munich Workshop on Design Technology Coupling

Thursday, June 30, 8:30am, till Friday, July 1, 2016, 4pm

Organizers: Helmut Graeb, TU Munich, Sani Nassif, Radyalis

Location: Technical University of Munich, Munich, Germany
Main Campus Munich, Arcisstr. 21, 80333 Munich
(exact room will be announced after registration deadline)

Registration: till June 1, 2016, by E-Mail to graeb@tum.de

PURPOSE:

The design of complex resilient systems requires an ever closer coupling of process variability and aging effects. Measuring process and operation deviations during manufacture and during lifetime, monitoring the function before and after manufacture, mitigating functional deviation through design and during operation are components of a resilient design that has to take place on all levels of abstraction.

This workshop is dedicated to an exchange among people from industry and academia working in this area. It includes contributions from the following collaborative projects:

- EUREKA-CATRENE RESilient Integrated SysTems, http://www.resist-catreneproject.eu/
- DFG Transregional Collaborative Research Center Invasive Computing, http://invasic.informatik.uni-erlangen.de
- DFG Priority Program SPP 1500 on Dependable Embedded Systems, http://spp1500.itec.kit.edu/

It is a one-time event to foster the exchange among the various people approaching resilient system design from low abstraction level, from high abstraction level, from academia, from industry, from methodic point of view, from application point of view. There will be *no workshop proceedings*, to enable an open discussion between participants.

The talks are either keynotes of 40 minutes length, followed by a 15 minutes Q&A, or talks of 14 minutes length in a group of consecutive talks w/o individual Q&A, followed by a 30 minutes panel and Q/A with all presenters in that group.

PROGRAMM THURSDAY, JUNE 30:

08:30

Opening

Helmut Graeb, Technical University of Munich

Welcome Note

Hartmut Hiller, Vice President Infineon, Design Enabling & Services

09:00

KEYNOTE: The Car of the Future will reinvent personal mobility

Patrick Leteinturier, Infineon Technologies, Automotive Systems

The regulations for CO2 and pollutant reduction have pushed the automotive industry for more electrification. The internal combustion engines will continue to power our vehicles for decades but will be assisted by electric traction in various xEV architectures. The race for efficiency, environment friendly, and safety will not end here. Automated and autonomous driving cars are opening a new field of benefits, but also a new field of challenges. The engineers will have to reinvent the EE vehicle architecture for new domain control and fail operational systems. The cars will be connected to other cars and the infrastructure with software update over the air. The new mobility will be real cyber physical system. This keynote will explore the potential of electronic technologies to solve the new requirements in sensing, controlling, powering, energizing the car of the future.

10:00

Coffee Break

10:30

KEYNOTE: Designing Closer to the Edge

Sani Nassif, Radyalis, USA

The economic imperative of the slowing down of Moore's law is a push on designers to get more of each succeeding technology node. Getting more relative performance from a technology requires (a) an understanding of the tolerances imposed by the process, (b) a characterization of the uncertainty imposed by variable operating conditions, and -importantly- (c) a recognition of the many "margins" inherently present in the design process. This talk reviews these concepts in the context of a foundry and IP-based future.

11:30

KEYNOTE: Optimizing Microprocessor Performance and Energy Efficiency through the use of on-chip sensors and integrated firmware control

Michael Floyd, IBM Systems Group, Austin/Texas, USA

Traditional guard banding of IC's leaves significant power efficiency and/or performance opportunity unrealized. As the performance benefits of transistor scaling continue to diminish, we can no longer afford to rely on a static operating voltage and fixed frequency while assuming worst case environmental conditions (noise and temperature). Techniques incorporating on-chip sensors and actuation, directed by integrated firmware control loops can continue to provide benefit as we squeeze more transistors into the same area.

12:30

Lunch Break

13:30

Dependable Embedded Systems – The DFG SPP 1500

Joerg Henkel, KIT, Karlsruhe

The talk gives a short introduction and overview of the DFG SPP 1500 Dependable Embedded Systems.

Reliable Runtime Reconfigurable Architectures

Lars Bauer, KIT, Karlsruhe

Dynamically reconfigurable architectures enable major acceleration of diverse applications by changing and optimizing the structure of the system at runtime. Permanent and transient faults threaten the correct operation of such architectures. This talk aims to show how to increase dependability of runtime reconfigurable systems by novel cross-layer strategies that (a) schedule self-tests at runtime, (b) prepare alternative implementations for the reconfigurable hardware (c)dynamically uses them to tolerate permanent faults and to mitigate aging, and (d) adaptively switch between different performance/redundancy trade-offs to mitigate soft errors.

Reliability Analysis and Optimization in the Presence of Uncertainty

Michael Glass, Friedrich-Alexander-University Erlangen-Nuernberg

Due to manufacturing tolerances and aging effects, future embedded systems have to cope with unreliable components. The intensity of such effects depends on uncertain aspects like environmental or usage conditions such that highly safety-critical systems are pessimistically designed for worst-case mission profiles. In this talk, we introduce a technique how to explicitly model the uncertain characteristics of system components, i.e. we model components using reliability functions with parameters distributed between a best and worst case. Since destructive effects like temperature may affect several components simultaneously (e. g. those in the same package), a correlation between uncertainties of components exists. The introduced uncertainty-aware method combines a formal analysis approach and a Monte Carlo simulation to consider uncertain characteristics and their different correlations. The approach can deliver a holistic view on the system's reliability with best/worst/average-case behavior and also insights on variance and quantiles. Since existing optimization approaches typically assume design objectives to be single values or to follow a predefined distribution. As a remedy, we present a dominance criterion for meta-heuristic optimization approaches like evolutionary algorithms that enables the comparison of system implementations with arbitrarily distributed characteristics.

Avoiding Residual Errors in Safety-Critical Many-Core Systems

Eberle Rambo, TU Braunschweig

Technology scaling increases the hardware susceptibility to transient and intermittent faults (soft errors), giving rise to the so-called unreliable hardware. Now, systems design for current and future technology have to cope with them. Techniques to overcome hardware induced errors in software execution can profit from the abundance of cores available in Multiprocessor Systems-on-Chip (MPSoCs) to increase reliability. The ASTEROID project proposes a real-time operating system design that provides reliable software execution by means of parallel redundant execution. Higher-level fault-tolerance mechanisms (e.g. replication) rely on a Reliable Computing Base (RCB), including parts of the hardware and the operating system. In this talk, we address the issue of avoiding residual errors when applying such systems to safety- and mixed-critical real-time systems, where stringent integrity and predictability requirements must be satisfied, with focus on the Network-on-Chip.

14:30

Panel with Presenters

15:00

KEYNOTE: TCAD based DTCO including variability and reliability

Asen Asenov, University of Glasgow and Gold Standard Simulations, Scotland, UK

Design-Technology Co-Optimization (DTCO) has become mandatory in advanced technology nodes. It is well understood that tailoring the transistor characteristics by tuning the technology is not sufficient any more. The transistor characteristics have to meet the requirement for design and optimization of particular circuits, systems and corresponding products. Modeling and simulation play an increasing important role in the DTCO process with the benefits of speeding up and reducing the cost of the technology, circuit and system development and hence reducing the time-to-market. In this talk we focus on DTCO co-optimization using on-purpose built and integrated DTCO tool chain that facilitates and significantly speeds up the simulation based DTCO process. We will provide illustrate the application of this approach with FinFET, FDSOI and NWT examples in the digital and the analogue design domain.

16:00

Coffee Break

16:30

KEYNOTE: Estimating Device-Parameter Variation using On-chip Sensitivity-Configurable Ring Oscillator

Masanori Hashimoto, Osaka University, Japan

This talk discusses how to estimate device-parameter variation for each fabricated chip, and introduces an area efficient device parameter estimation method with on-chip sensitivity-configurable ring oscillator (RO). This sensitivity-configurable RO has a number of configurations and the proposed method exploits this property for estimating individual device parameters, reducing sensor area and/or improving estimation accuracy. This talk explains how to find a good set of sensitivity configuration with small prospective error, and proposes to select multiple sets of sensitivity configurations and obtain multiple estimates for accuracy improvement exploiting an averaging effect. Experimental results with a 32-nm predictive technology model show that the proposed method can successfully estimate parameter variations of channel length and threshold voltage variation.

17:30

Invasive Computing - The DFG Transregional Research Center 89

Juergen Teich, Friedrich-Alexander-University Erlangen-Nuernberg

The talk gives a short introduction and overview of topic and the research and benefits of invasive multi-core computing.

Providing Fault Tolerance Through Invasive Computing

Vahid Lari, Friedrich-Alexander-University Erlangen-Nuernberg

In this talk, we present techniques for providing on-demand structural redundancy for Coarse-Grained Reconfigurable Arrays (CGRAs) and a calculus for determining the gains of reliability when applying these replication techniques inspired by invasive computing from the perspective of safety-critical parallel loop program applications. Here, for protecting massively parallel loop computations against errors like soft errors, well-known replication schemes such as Dual Modular Redundancy (DMR) and Triple Modular Redundancy (TMR) must be applied to many Processor Elements (PEs)rather than one based on application requirements for reliability and Soft Error Rates (SERs). Moreover, different voting options and signal replication schemes are investigated. It will be shown that hardware voting may be accomplished at negligible hardware cost, i. e., less than two percent area overhead per PE, for a class of reconfigurable processor arrays called Tightly Coupled Processor Arrays (TCPAs). As a major contribution of this paper, a formal analysis of the reliability achievable by each combination of replication and voting scheme for parallel loop executions on CGRAs in dependence of a given SER and application timing characteristics (schedule) is elaborated. Using this analysis, error detection latencies may be computed and proper decisions which replication scheme to choose at runtime to guarantee a maximal probability of failure on-demand can be derived. Finally, fault-simulation results areprovided and compared with the formal analysis of reliability.

On-Chip Diagnosis of Multicore Platforms for Power Management

Mark Sagi, Technical University of Munich

Power and energy efficiency are of ever increasing importance for multicore processors. Processor cores have to be operated in a way that both the application processing requirements and the thermal constraints are met. In this talk, we present our ideas and concepts to assist power management by a diagnosis layer which enables the identification of power inefficiencies for the novel invasive computer architecture. We discuss how to consolidate on chip sensor data in combination with application specific knowledge to derive optimal power management decisions. These range from conventional DVFS to predictively darkening cores with the goal of decreasing power inefficiencies and thermal stress.

18:15

Panel with Presenters

18:45

Get Together

PROGRAMM FRIDAY, JULY 1:

08:30

KEYNOTE: Cross-Layer Reliability Monitoring, Margining and Mitigation

Puneet Gupta, University of California at Los Angeles, USA

Increased variability, wearout and failure modes have created new challenges for conventional hardware guardbanding,as the additional design margin diminishes the benefits of technology scaling. This talk discusses cross-layer approaches to reduce total system design margin.
We start by proposing two different types of performance monitors that can achieve better monitoring accuracy and smaller monitoring overhead. We also demonstrate the use of these performance monitors in system adaptation with our end-to-end implementation of software testbeds. We also study the dynamic variation and reliability margining problem emerging system contexts. In a system with monitor-and-actuate adaptation, dynamic variations require extra margin for monitor and actuate latencies. We analyze and study the margining problem considering different choices of the monitor and actuator types. System reliability margining strategies are also proposed for circuits in the "dark silicon" era, where the low-level design margin should consider the contexts of high-level power/thermal constraints. We study the impacts of dynamic power management schemes on system reliability through an emulation platform. Lastly, we propose a clock gating methodology to mitigate the aging induced clock skew, which is difficult to monitor and resolve through adaptation.

09:30

KEYNOTE: Taking Control of On-chip Process and Thermal Variations: From Sensors and Models to Runtime Management Techniques

Sherief Reda, Brown University, Providence/Rhode Island, USA

On-chip variations arising from process variability and runtime thermal gradients have a major impact on the aging and reliability of integrated circuits. In this talk, I will first describe experimental techniques to quantify the magnitude of process variability and thermal variations of integrated circuits. To enable runtime control, I will provide designs for embedded sensors that can monitor process variability and thermal variations at strategic locations on the chip. I will then discuss mathematical models that leverage the measurements from the embedded sensors to devise chip-level estimations beyond the locations of the sensors. Finally, I will describe how to design feedback controller systems that monitor the sensor measurements or the models and use their outcomes to dynamically adjust the degrees of freedom in the chip (e.g., voltage/frequencies or cooling capacity) to ensure reliable operation. Measurements and results from a number of real processors and programmable devices will be presented.

10:30

Coffee Break

11:00

Safe Operating Region Prediction Through Simulation

Fulvio Schiappelli, Dialog Semiconductor

In DC/DC switching voltage regulators it proves essential to estimate the degradation of the power switch devices (usually NLDMOS transistors), in order to avoid unnecessary oversizing and consequent wasting of silicon area. The most common mechanisms responsible for degradation of the switches performance (and even self-destruction) are junction breakdown due to avalanching and hot-carrier injection. The silicon manufacturer provides SOA (Safe Operating Area) curves for each power device available in the process, which guide the circuit designer in choosing and biasing the power switches properly for the given application. This presentation shows that, combining SOA curves with simulations, the expected lifetime of a power switch can be predicted and the device size can be accurately tuned, to save silicon area without compromising on performances.

Charge based design method for CMOS circuits

Steffen Paul, Uni Bremen

Due to the shrinking feature sizes within modern CMOS technology nodes a number of physical effects nowadays influence the device behavior in such a way, that it is noticeable within the functionality of the overall system. These effects can either result from the manufacturing process, from the circuits' operating time respectively conditions or from external factors such as radiation and temperature. What all these effects have in common as an indicator is a raise of the transistors threshold voltage. This raise leads to changes of the characteristics of each single transistor and may cause a push of the systems overall functionality to the outside of the systems' specification boundaries. This contribution presents a design approach for modern CMOS circuits simply based on the simulation of one NMOS and one PMOS device for the chosen technology node. The presented approach can be set up based onto any kind of transistor model so that especially detailed transistor models

taking charge effects at the physical level into account can be used as a basis for the overall system design process. This way it becomes possible to also find out about the cause for the change in the threshold voltage. The strengths as well as the weaknesses of the chosen approach will be demonstrated based on two illustrating examples: a low noise amplifier and a beta multiplier circuit.

11:30

Panel with Presenters

12:00

Lunch Break

13:00

Device Parameter Extraction for Aging Model Evaluation – Test Window Gaps affect Model Validation

Andreas Aal, Volkswagen, Braunschweig

The ongoing increase of semiconductor technology complexity through scaling, 3D integration and inclusion of more and more new materials within the IC stack are the result of the industries' approach to stay competitive (Moore's Law). However, with the increasing need to provide more robust devices to automotive, automation, avionics and the IoT market in general, design gaps between original mass volume products and new application fields become more evident. Unfortunately, these design gaps are not limited to functional aspects. It turns out that degradation, aging, and behavior under severe environmental and operation conditions are virtually Terra Incognita. They have not been investigated due to cost optimization processes regarding focused design targets in the communication and consumer business. In this presentation, we show exemplary results on the effect of thermomechanical and other stress on the outcome of the parameter extraction process on primitive device modelling that is fundamental for any model based verification of IC designs in advanced nodes.

Starting the journey towards resilient automotive electronics

Franz Dietz, Bosch

In future cars electronics take over more and more responsibility for the safety of the driver and its environment. For advanced driver assistance systems or even autonomous driving, improved safety and reliability are the key: From an end-customer point of view recent news concerning field failures and recalls due to electronics reduce the trust of customers in technology.

The industry must find ways to improve the reliability and trust in the electronic systems, especially for highly integrated semiconductor technologies. A possible solution is the introduction of resilient automotive systems, which will be discussed during the presentation. The resulting confidence in technology will be a crucial point for market acceptance of modern driver assistance systems and introduction of autonomous driving.

Tbd

Vincent Huard, ST Microelectronics

13:45

Panel with Presenters

14:15

KEYNOTE: Natural Solutions to Electronic Systems Design Problems

Martin Trefzer, York University, UK

The increasing versatility, performance, compactness and power efficiency of today's electronic systems is achieved by pushing technology to its physical limits: systems are increasing in size and complexity comprising thousands of subsystems made of billions of devices, requiring sophisticated programming and control; the devices themselves become smaller and smaller and have reached the atomic scale, which leads to stochastic variations when fabricating them. This makes components more noisy and unreliable and designing reliable systems extremely challenging. In this respect, technological systems are far behind biological organisms which have long since accomplished the feat of not only operating reliably with highly variable components, but also maintaining and tuning themselves in changing environments, when faults occur or they are otherwise perturbed. Biological mechanisms enabling this have co-evolved with the organisms, hence, are perfectly adapted to the requirements of their embodiment. In this context, evolutionary hardware is about hardware that offers the capability to change its structure and behaviour in order to automatically optimise its operation for a specific task or environment, taking inspiration from biological organisms with natural evolution as nature's guiding optimisation principle. In the talk I will give examples of evolutionary computation applied to

electronic design optimisation and performance analysis, and how bio-inspired decision making can improve throughput and fault tolerance of networks on chip.

15:00

Poster Session

16:00

Closing

BIOS (ALHABETICAL ORDER):

Andreas Aal

Andreas Aal joined Volkswagen AG, Wolfsburg, Germany, in 2011 with focus on Semiconductor Reliability Assurance (technical development) in Automotive Applications. Now, being responsible on corresponding strategic and operational levels, his activities concentrate on technology capability enhancement of nodes down to 14 nm for automotive applications. He leads two semiconductor related European projects and is a representative of the through-the-supply-chain-joint-development approach. Mr. Aal has been working within the Semiconductor Industry holding different positions from Engineering to Management (Process Engineer, Wafer FAB Project Manager for Process Build-in-Reliability Development, Global Reliability Assurance Manager) working on plasma-damage, failure analysis, production monitoring and process and technology qualification. He was involved in the development of test structure design as well as new combined stress/measurement and data analysis methodologies for qualification and fWLR monitoring on the topics: dielectrics, plasma induced damage and metallization. He accompanied several reliability growth projects and influenced process and technology design for 1.2 um to 0.18 um nodes for both in-house and foundry manufacturing. Andreas (certified reliability professional) has published and co-authored various papers, has served as reviewer for different journals and has served in the technical and management committee for IEEE IIRW. He is a member of the IEEE Electron Devices, CPMT, Nuclear and Plasma Sciences, Reliability and Solid-State Circuits Societies and also a frequent participant/contributor of the JEDEC subcommittee 14.2. Since 2007 he is chair of the German ITG group 8.5.6 (VDE) on (f) WLR, reliability simulations and qualification.

Asen Asenov

Asen Asenov (FIEEE, FRSE) is a founder and CEO of Gold Standard Simulations (GSS) Ltd. (www.goldstandardsimulations.com). GSS is the leader in predictive simulation of performance and of statistical variability in advanced CMOS, compact model extraction and generation technology and statistical circuit simulation. The GSS customers include foundries, IDMs, and fables companies. Asenov is also a Director of SureCore, Ltd, a low power SRAM design IP start-up company, SemiWise, Ltd. a semiconductor device IP company and Ngenics, Ltd an EDA tools development company. As a James Watt Professor in Electrical Engineering and Leader of the 30 members strong Glasgow Device Modelling Group (http://web.eng.gla.ac.uk/groups/devmod/) Asenov directs the development of 2D and 3D quantum mechanical, Monte Carlo and classical device simulators and their application in the design of advanced and novel CMOS devices. Asenov has more than 750 publications and more than 170 invited talks in the above areas. For more details please see: http://scholar.google.co.uk/citations?user=owyRYmMAAAAJ&hl=en.

Lars Bauer

Lars Bauer received his M.Sc. and Ph.D. (Dr.-Ing.) in Computer Science from the University of Karlsruhe, Germany in 2004 and 2009, respectively. He is currently a research assistant, lecturer and group leader at the Chair for Embedded Systems (CES) at the Karlsruhe Institute of Technology (KIT). His main research interests are reconfigurable and adaptive computing systems. He received the EDAA Outstanding Dissertations Award, the FZI Outstanding Dissertations Award, and best paper awards at AHS'11 and DATE'08. Dr. Bauer is a principal investigator at the "Invasive Computing" research initiative and the KIT Young Investigator Group "Methods and Architectures for emerging dynamically reconfigurable systems".

Franz Dietz

Franz Dietz studied microsystem technology at the University of Applied Science in Regensburg. From 1999-2011 he worked at Atmel Germany and Telefunken Semiconductors, leading the department of process characterization and process development. He has authored or co-authored several papers on SOI smart power technologies and contributed to more than 20 patents for integrated silicon-devices and technologies. Franz Dietz joined Bosch's department for Automotive Electronics in 2011, being responsible for the introduction of modern smart power technologies. Since 2015 he is involved in the European project RESIST as work package leader for "Integrated failure detectors and diagnostic solutions".

Michael Floyd

Michael Floyd received a Bachelor's degree in Computer Engineering with highest honors from the Georgia Institute of Technology in 1995 and a Master's degree in Electrical Engineering from Stanford University in 2000. Michael is the recognized technical leader and expert for IBM Systems in the area of Power Management, where he has served as the power management design architect and team lead for the last three POWER chip designs. He was a founding member of EnergyScale (a term which he created & had trademarked for IBM) and the team of engineers spanning the processor, system, and firmware development to deliver this customer offering. In 2012, Michael spearheaded the successful adoption of CPMs (Critical Path Monitors) on P7+ systems to gain both a 2% benchmark boost and significant energy efficiency gains by incorporating a novel new circuit guardbanding technique. The CPM mechanism was also used to protect against voltage droops on other products and was instrumental in shipping the IBM P775 Supercomputer (HPC machine based on POWER7) and z13 (Mainframe) at full frequency with acceptable yields due to the reduced circuit power. In addition to energy management, Michael has a broad and unique set of skills and experience in the area of microprocessor & chip design that he has leveraged to deliver cutting-edge design features and has left his mark on several critical areas of the machine, beginning with POWER4. His contributions span: "pervasive" (RAS, test, bringup, and debug) design infrastructure including "design for debug" (built-in trace arrays and logic analyzer), which is now implemented in every chip IBM makes; Elastic Interface custom implementation, timing methodology, and interface test; Concurrent Server Maintenance; cycle-reproducible and cache-contained test exerciser for use as a manufacturing test and debug tool; performance monitoring & tracing; on-chip analog timing and temperature sensors; Core Multi-threading and Idle (Power Managed) State architecture. More recently Michael's innovations have included using an embedded microcontroller as a "tester on a chip" for reduce manufacturing test time, as well as the architecture and implementation of a new lightweight PowerPC micro-controller (that has been dubbed the "PPE" engine) on IBM's chips that will be instrumental in the boot and runtime control of all future IBM systems. Michael is recognized by IBM as a Master Inventor, where his prolific IP has protected these emerging areas of innovation that have key competitive advantage and value-add. He also has published and presented a number of technical articles on these topics in premier industry publications and conferences. Since 2006 he has been an STG mentor/advocate for IBM research teams in both Austin and Watson Research Labs, with whom he works closely.

Michael Glass

Michael Glaß holds an assistant professorship for Dependable Embedded Systems and heads the System-level Design Automation group at Hardware/Software Co-Design, Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany. He received his Diploma degree and Doctorate degree in computer science from the FAU, Germany, in 2006 and 2011, respectively. Michael's research interests are dependability engineering for embedded systems and system-level design automation with particular focus on formal analysis and design space exploration.

Puneet Gupta

Puneet Gupta (http://nanocad.ee.ucla.edu) is currently a faculty member of the Electrical Engineering Department at UCLA. He received the B.Tech degree in Electrical Engineering from Indian Institute of Technology, Delhi in 2000 and Ph.D. in 2007 from University of California, San Diego. He co-founded Blaze DFM Inc. (acquired by Tela Inc.) in 2004 and served as its product architect till 2007.

He has authored over 130 papers, 16 U.S. patents, a book and a book chapter. He is a recipient of NSF CAREER award, ACM/SIGDA Outstanding New Faculty Award, SRC Inventor Recognition Award and IBM Faculty Award. He currently leads the IMPACT+ center (http://impact.ee.ucla.edu) which focuses on future semiconductor technologies.

Dr. Gupta's research has focused on building high-value bridges across software-hardware-technology interfaces for lowered cost and power, increased yield and improved predictability of integrated circuits and systems.

Masanori Hashimoto

Masanori Hashimoto received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Now, he is a Professor with the Department of Information Systems Engineering, Osaka University, Osaka, Japan. His current research interests include computer-aided design for digital integrated circuits, design for manufacturability and reliability, timing and power integrity analysis, and low-power circuit design.

Dr. Hashimoto was a recipient of the Best Paper Award at ASP-DAC 2004. He was on the technical program committees of international conferences including DAC, ICCAD, ITC, Symposium on VLSI Circuits, ASP-DAC and DATE. He currently serves as an associate editor for IEEE Transactions on VLSI Systems and Circuits and Systems I.

Joerg Henkel

Prof. Jörg Henkel is currently with Karlsruhe Institute of Technology (KIT), Germany, where he is directing the Chair for Embedded Systems CES. Before, he was a Senior Research Staff Member at NEC Laboratories in Princeton, NJ. He received his PhD from Braunschweig University with "Summa cum Laude". Prof. Henkel has/is organizing various embedded systems and low power ACM/IEEE conferences/symposia as General Chair and Program Chair and was a Guest Editor on these topics in various Journals like the IEEE Computer Magazine. He was Program Chair of CODES'01, RSP'02, ISLPED'06, SIPS'08, CASES'09, Estimedia'11, VLSI Design'12, ICCAD'12, PATMOS'13, NOCS'14 and served as General Chair for

CODES'02, ISLPED'09, Estimedia'12, ICCAD'13 and ESWeek'16. He is/has been a steering committee member of major conferences in the embedded systems field like at ICCAD, ESWeek, ISLPED, Codes+ISSS, CASES and is/has been an editorial board member of various journals like the IEEE TVLSI, IEEE TCAD, IEEE TMSCS, ACM TCPS, JOLPE etc. In recent years, Prof. Henkel has given around ten keynotes at various international conferences primarily with focus on embedded systems dependability. He has given full/half-day tutorials at leading conferences like DAC, ICCAD, DATE etc. Prof. Henkel received the 2008 DATE Best Paper Award, the 2009 IEEE/ACM William J. Mc Calla ICCAD Best Paper Award, the Codes+ISSS 2015, 2014, and 2011 Best Paper Awards, and the MaXentric Technologies AHS 2011 Best Paper Award as well as the DATE 2013 Best IP Award and the DAC 2014 Designer Track Best Poster Award. He is the Chairman of the IEEE Computer Society, Germany Section, and was the Editor-in-Chief of the ACM Transactions on Embedded Computing Systems (ACM TECS) for two consecutive terms. He is an initiator and the coordinator of the German Research Foundation's (DFG) program on 'Dependable Embedded Systems' (SPP 1500). He is the site coordinator (Karlsruhe site) of the Three- University Collaborative Research Center on "Invasive Computing" (DFG TR89). He is the Editor-in-Chief of the IEEE Design&Test Magazine since January 2016. He holds ten US patents and is a Fellow of the IEEE.

Vahid Lari

Vahid Lari is a post-doctoral researcher at the Chair for Hardware/Software Co-Design at Friedrich-Alexander University Erlangen-Nürnberg (FAU), Germany. He received a bachelor degree in computer engineering in 2005 from University of Isfahan, Iran, a master degree in computer architectures in 2007 from Sharif University of Technology, Iran, and a PhD degree (Dr.-Ing.) from Friedrich-Alexander University Erlangen-Nürnberg, Germany, in 2015. His main research interests include fault tolerance, programmable hardware accelerators, the design of massively parallel architectures, system level performance evaluation.

Patrick Leteinturier

Patrick Leteinturier received a Mechanical Engineering degree from ENSAM: Ecole Nationale Supérieure des Arts et Métiers (France) in 1987, a Master of Advanced Studies in Internal Combustion Engines (DEA) at the University Paris 6 (France), and an Electric & Electronic Engineering degree from ESE: Ecole Supérieure d'Electricité (France) in 1990. Between 1990 and 1999, Patrick Leteinturier worked as development engineer at JV Lucas (UK) & SAGEM (France) for engine management systems, as chief engineer at SAGEM (France) in charge of PSA and Renault Powertrain projects, and as development engineer at Siemens-Semiconductor for automotive 32bit TriCore µC. Since 1999 he is with Infineon Technologies, since 2013 as Automotive System Technical Fellow. He is responsible for system architecture of silicon products (silicon sensors, microcontrollers, silicon smart powers, and power modules) for Engine, Transmission and xEV applications. A member of SAE International since 1998, Mr. Leteinturier received the SAE International Forest R. McFarland Award (2008). In 2010, he was named an SAE International Fellow. Mr. Leteinturier is currently SAE director and member of the SAE Engineering Meeting Board. Mr. Leteinturier is Guest Professor Tianjin University in China (since 2006).

Sani Nassif

Sani received his PhD degree from Carnegie-Mellon University in 1986, then worked for ten years at Bell Laboratories in the general area of technology CAD. In January 1996, he joined the IBM Austin Research Laboratory (ARL), which was founded with a specific focus on research for the support of IBM's Power computer systems. After twelve years of management, he stepped down to focus on technical work again with an emphasis on applying techniques developed in the VLSI-EDA area to IBM's Smarter Planet initiative. In January 2014 Sani founded Radyalis, a company focused on applying VLSI-EDA techniques to the field of Cancer Proton Radiation Therapy. Sani has authored one book, many book chapters, and numerous conference and journal publications. He has delivered many tutorials at top conferences, received many Best Paper awards, and has given many Keynote and Plenary presentations. He is an IEEE Fellow, was a member of the IBM Academy of Technology, a member of the ACM and the AAAS, and an IBM master inventor with more than 75 patents.

Steffen Paul

Steffen Paul studied electrical engineering at Technical University Dresden and Technical University Munich from 1984-1989, where he received his Diploma (Dipl.-Ing.) degree in 1989. From 1989-1997 he was working at the Institute of Network Theory and Circuit Design of the same institution. In 1993 he received the Dr.-Ing. degree. He held a postdoctoral position at the EECS department of the University of California, Berkeley in 1994-1995. From 1997-2007 he was working at Infineon Technologies (former Siemens Semiconductor group) in the areas of memory design, xDSL and UMTS concept engineering. He joined the University Bremen in 2007 as a full professor for electromagnetic theory and microelectronic systems. His research interests include signal processing for wireless communications, VLSI implementation of signal processing algorithms and low power digital design.

Eberle Rambo

Eberle A. Rambo received the Bachelor and Master degrees in Computer Science at the Federal University of Santa Catarina, Brazil, in 2009 and 2011, respectively, and is currently a PhD candidate in Computer Engineering at Technische Universität Braunschweig, Germany. His current research interests are real-time systems, focusing on the reliability and predictability of many-cores and Networks-on-Chip.

Sherief Reda

Sherief Reda is an Associate Professor at the School of Engineering, Brown University. He joined the Computer Engineering group at Brown in 2006 after receiving his Ph.D. in computer science and engineering from University of California, San Diego. His general research interests are in the area of computer engineering, with focus on energy-efficient computing, thermal-power sensing, modeling and management, and variability-aware physical design. Professor Reda received a number of research awards and acknowledgments, including a best paper award in DATE 2002, a hot article in Operations Research letters in 2004, a first place award in ISPD VLSI placement contest in 2005, best paper nominations in ICCAD 2005 and ASPDAC 2008, a NSF CAREER award in 2010, a best paper award in ISLPED 2010 and a best paper nomination in 2015. He is a senior member of IEEE.

Mark Sagi

Mark Sagi is working towards the PhD degree at Technical University of Munich (TUM) since 2016. He received his BS and MS degrees in electrical engineering and information technology from TUM in 2013 and 2015, respectively. His research interests are on power monitoring and self-adaptive power management for multicore SoCs.

Fulvio Schiappelli

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