

# Neue Möglichkeiten schaffen – Europäische Intel Forschung für Visual Computing, Exascale und Paralleles Rechnen

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Systems Group



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# Gliederung

- Intel Forschung in Europa
  - Intel Labs Europe
- Visual Computing
  - Intel Visual Computing Institute, Saarbrücken
- Paralleles Rechnen
  - Concurrent Collections und paralleles JavaScript
- HPC und Exascale
  - Herausforderung Exascale
  - Intel European Exascale Labs

**INTEL FORSCHUNG IN EUROPA**

# Intel Corporation:

## *The World's Largest Semiconductor Manufacturer*

- Leading Manufacturer of Computer, Networking & Communications Products
- 168 Sites and 578 Buildings in 63 Countries
- \$54B in Annual Revenues from Customers in Over 120 Countries
- 25 Consecutive Years of Positive Net Income
- Over 100,000 Employees
- 80,000 technical roles, **10,400 Masters in Science**, **5,200 PhD's**, 4,000 MBA's
- One of the Top Ten Most Valuable Brands in the World for 11 Consecutive Years
- Ranked #46 on Fortune's 100 Best Companies to Work For List
- Invests \$100 Million Each Year in Education Across More than 70 Countries
- The Single-Largest Voluntary Purchaser of Green Power in the United States
- More than One Million Hours of Volunteer Service in Our Communities in 2011



# Intel Labs

*Delivering Breakthrough Technologies to Fuel Intel's Growth*



## Strong Research Partnerships

UNIVERSITIES



GOVERNMENT



INDUSTRY



## World Class Research



Processing & Programming



Energy & Sustainability



Security & Virtualization



Si Photonics & Wireless

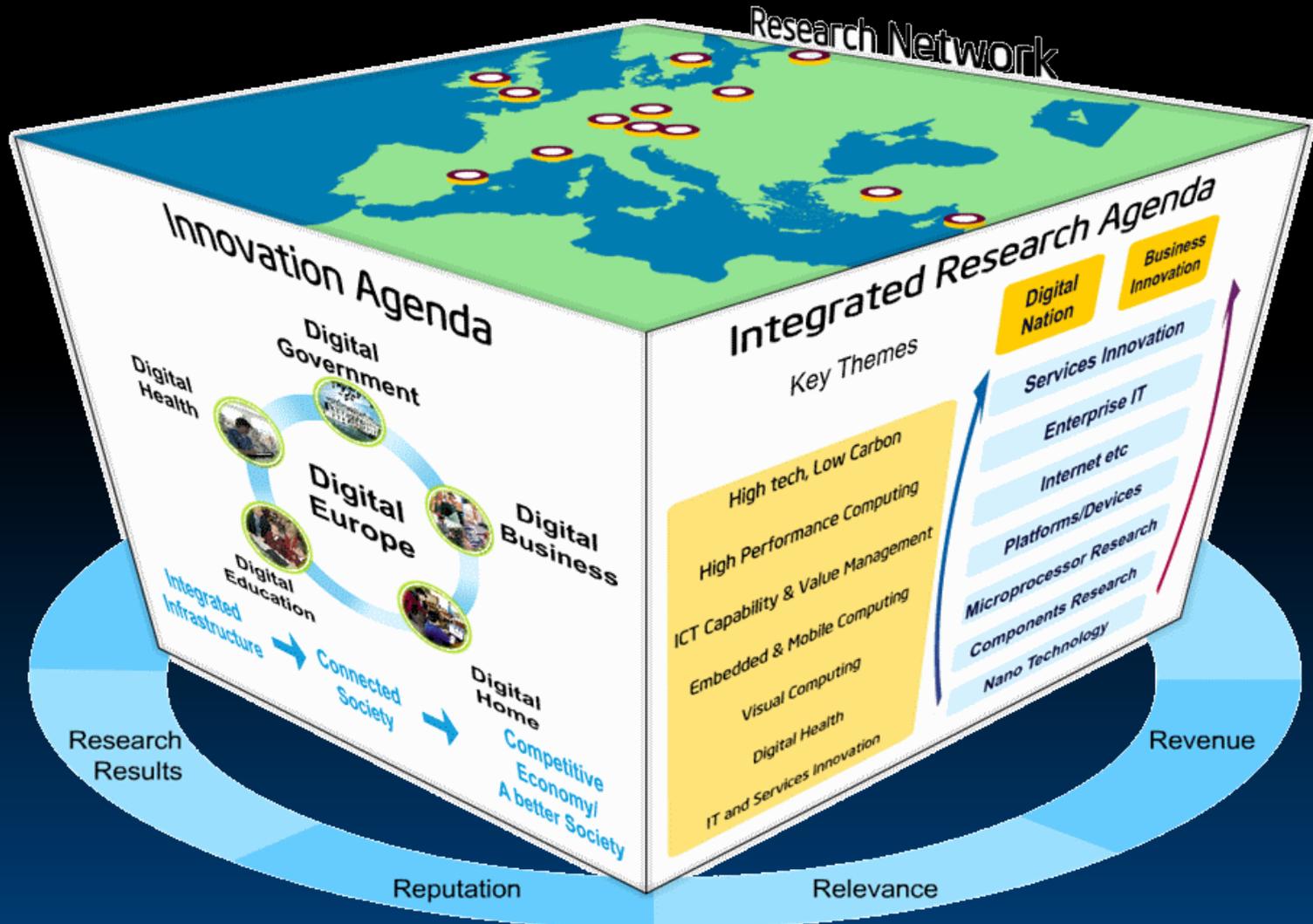


User Experience & Interaction

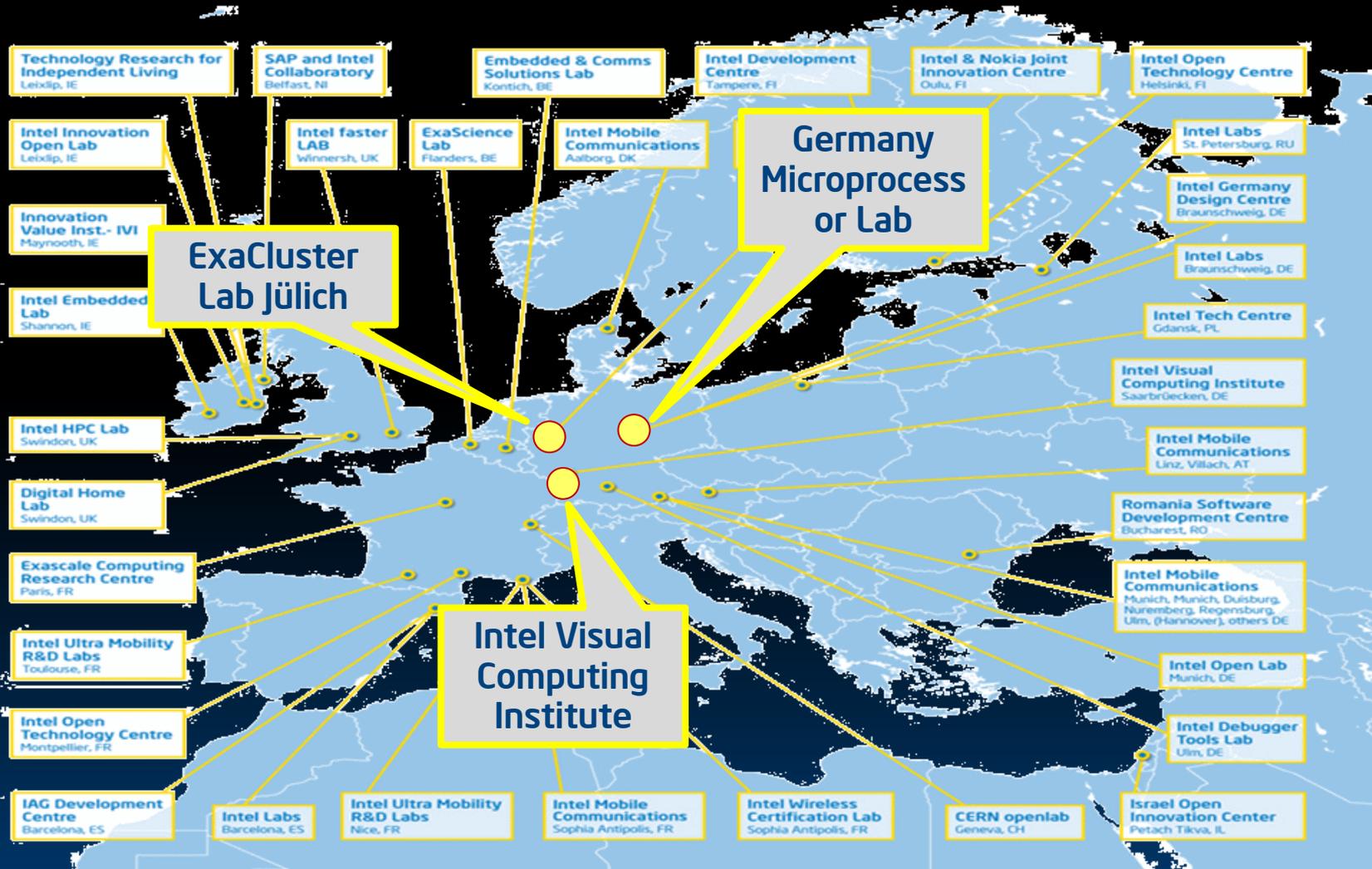
*... and much more!*



# Intel Labs Europe Innovation and Research



# ILE Network



# VISUAL COMPUTING

# Intel Visual Computing Institute

- Kooperation von Intel Labs, Universität des Saarlandes, DFKI, MPI für Informatik, MPI für Softwaresysteme
- Kofinanzierung von Forschungsprojekten
- Zur Zeit 50 Forscher/innen, 19 Projekte
- Nächster RfP in für Mitte 2012 geplant
- Offen für alle Forschungspartner in Europa

<http://www.intel-vci.uni-saarland.de/>



VISUAL  
COMPUTING  
INSTITUTE



UNIVERSITÄT  
DES  
SAARLANDES



max planck institut  
informatik



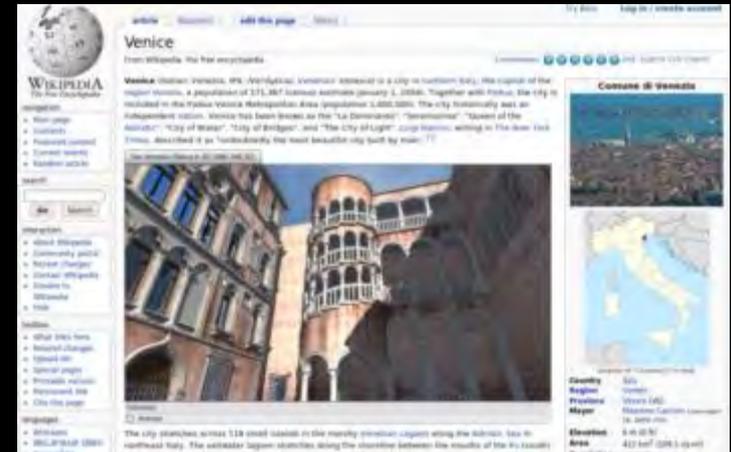
Max  
Planck  
Institute  
for  
Software Systems



# IVCI Projekte – Interactive 3D Web Content

Prof. Philipp Slusallek, DFKI

- XML3D Scene Description
  - XHTML5 extension
  - Built into the browser
  - Supports Web APIs (DOM\*, CSS, JS\*\*)
- XFLOW Workflow Description
  - Parallel data processing
  - Fully programmable pipeline
  - Accessible from DOM
- Results
  - Firefox and Chromium demonstrators
  - W3C standardization



\*Domain Object Model  
\*\*JavaScript

[www.xml3d.org](http://www.xml3d.org)



# IVCI Projekte – Markerless Performance Capture

Prof. Christian Theobalt, MPI Informatik

- Reconstruction of detailed human animation models
  - In: Multi-view video without markers
  - Out: Detailed motion, shape and appearance
  - General clothing, modifiable performances, new animations



- Real-time performance capture
  - Fast full-body motion estimation from depth cameras
  - Interaction
  - Virtual mirror



VISUAL  
COMPUTING  
INSTITUTE



UNIVERSITÄT  
DES  
SAARLANDES



max planck institut  
informatik



Max  
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Institute  
for  
Software Systems



# Embree Photo-Realistic Ray Tracing Kernels

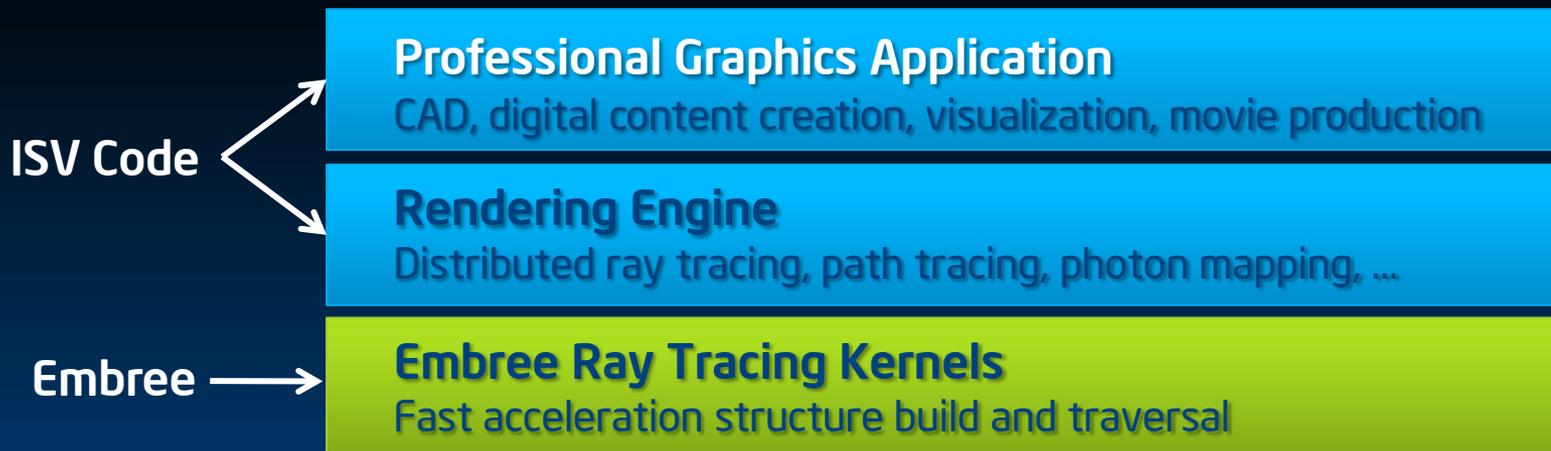
Dr. Manfred Ernst, Intel

## What is Embree?

- The fastest ray tracing kernels for Intel® CPUs
- A photo-realistic renderer for demo purposes

## Integrating Embree

- Replaces a small component of ISV code
- Has a large performance impact



# Embree Photo-Realistic Ray Tracing Kernels

Dr. Manfred Ernst, Intel



1000 x 1200 pixel, rendered on four Intel® Xeon® Processor E7-4860  
Model courtesy of Martin Lubich, [www.loramel.net](http://www.loramel.net)

- Source code and example scenes freely available at <http://software.intel.com/en-us/articles/embree-photo-realistic-raytracing-kernels>



# PARALLELES RECHNEN

# Intel Software Development Tools

## Choice of parallel programming models

- OpenMP\*
  - Pragma- based approach to threading geared towards array—dominated processing
- Intel® Cilk™ Plus
  - C/C++ language extensions enable simple, task-based programming
  - New: comprehensive notation for array operations simplifies SIMD programming
- Intel® Threading Building Blocks
  - Generic implementations of parallel performance patterns, concurrent data structures, sync primitives and scalable memory allocators
- Intel® MPI Library
  - Highly scalable message-passing library for distributed memory systems, excellent performance and adaptability

## Coming up

- OpenCL\* for explicit offload programming
- Offload pragmas for MIC

```
#pragma omp parallel for
for (i=0; i<N; i++)
    Foo(array[i]);
```

```
cilk_spawn qsort(begin, middle);
qsort(middle+1, end);
cilk_sync;
```

```
if (mask[i])
    a[i] = b[i] + m[i];
m[i] = foo(a[i]);
```

```
tbb::concurrent_queue<int> q;
MyType<char, tbb::tbb_allocator<char>> data;
Tbb::parallel_sort(data.begin(), data.end());
```

```
MPI_Send(&a[0], count, MPI_FLOAT, dest, tag,
        MPI_COMM_WORLD);
MPI_Reduce(&b, &sum, 1, MPI_FLOAT, MPI_SUM,
        MPI_COMM_WORLD);
```

<http://software.intel.com/en-us/intel-sdp-home/>



# Concurrent Collections

Frank Schlimbach, Intel

Conventional (distributed memory) models require

- Specification which operations must run in parallel
- Mapping of these to hardware resources

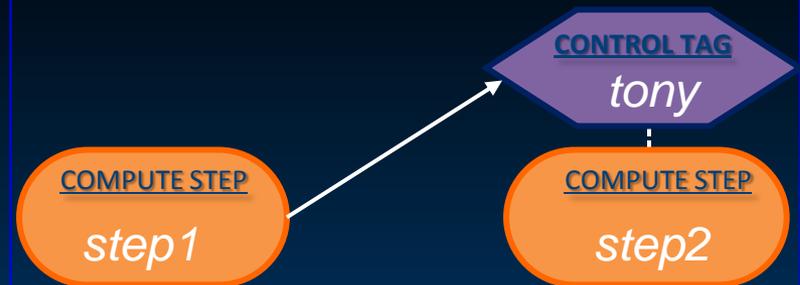
For CnC, all that's necessary is

- Specification of the *semantic ordering* constraints

Producer - Consumer



Controller - Controllee



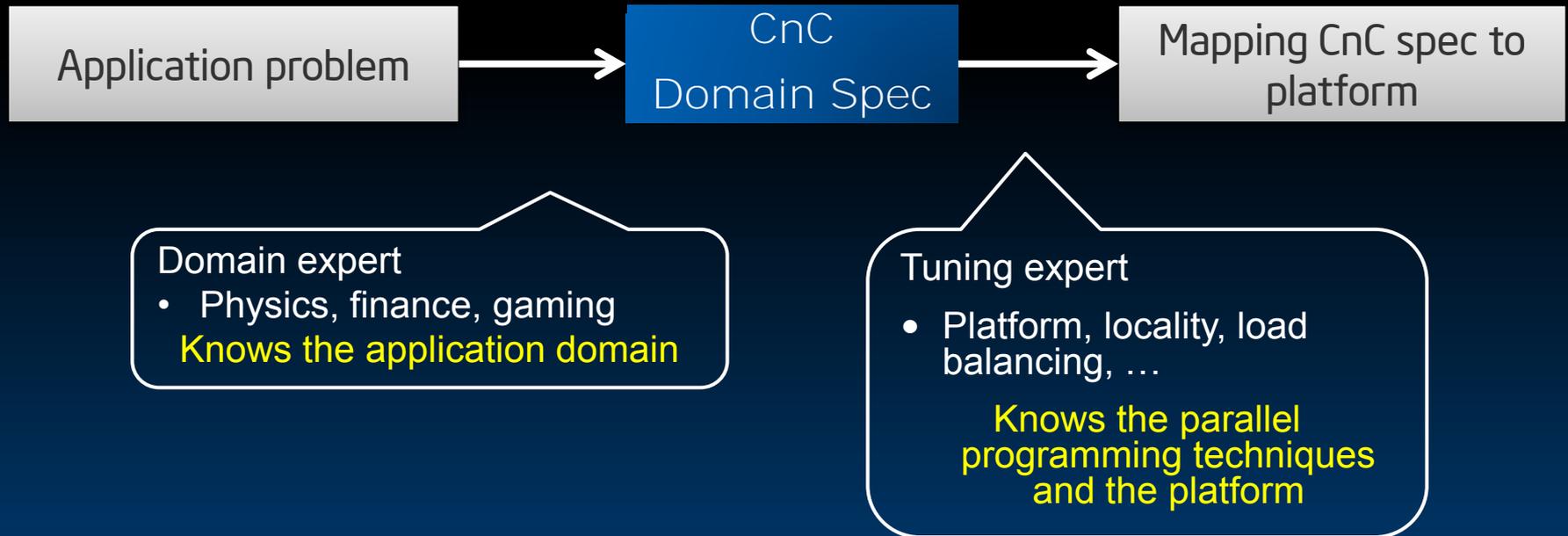
# Concurrent Collections

Frank Schlimbach, Intel

CnC is a coordination language

- Works together with a compute language (C++, Java, Python, Scala, ...)

Facilitates separation of concerns



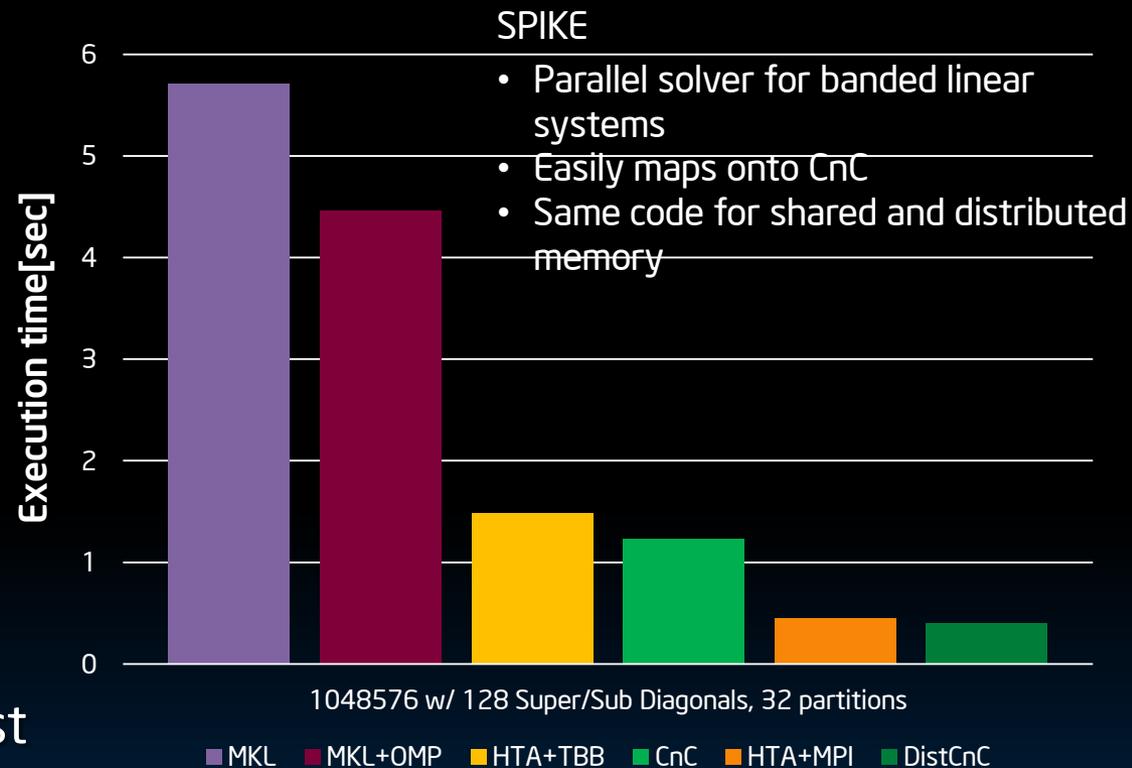
# Concurrent Collections

Frank Schlimbach, Intel

(Surprisingly) good performance

Support for distributed memory

- Data distribution orthogonal to everything else
- Can tune distributions without disturbing the rest of the code



<http://software.intel.com/en-us/articles/intel-concurrent-collections-for-cc/>

<http://habanero.rice.edu/cnc>



# River Trail: Parallel Javascript

Tatiana Shpeisman, Intel

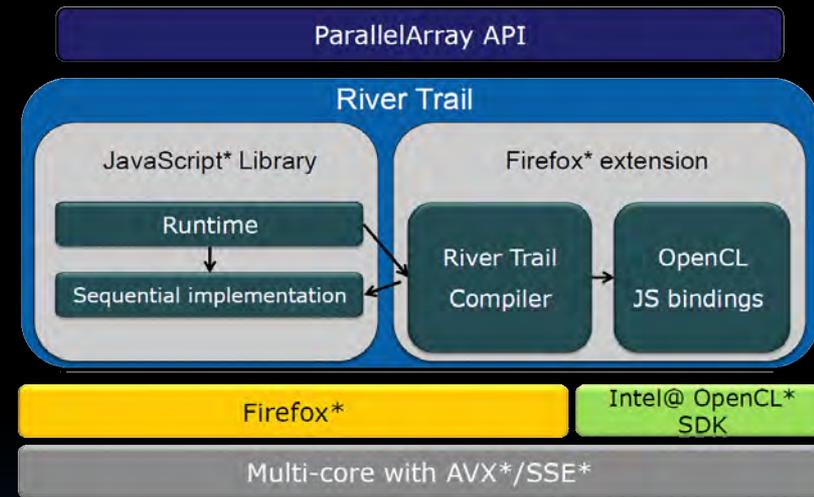
- Javascript executes sequentially – takes no advantage of multicore hardware
- Web Workers implements low level, thread based model
  - Parallel programming the hard way ...
- River Trail extends Javascript language by *data parallelism*
  - Concurrent, independent operations on elements of parallel arrays
  - Runtime system maps to parallel HW and devises schedules
  - Deterministic execution, no race conditions, no deadlock



# River Trail: Parallel Javascript

Tatiana Shpeisman, Intel

- New `ParallelArray` data structure
  - Immutable, dense, homogeneous
- Six methods provide basic skeletons for parallel computing
  - **Map, combine, reduce, scan, filter, scatter**
- Side-effect free elemental functions
  - Compute one element of the array



<https://github.com/RiverTrail/RiverTrail>

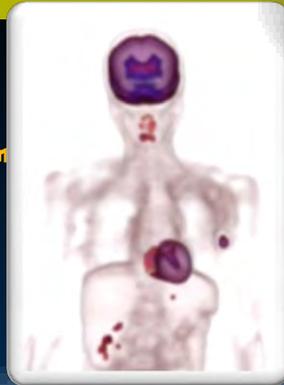
# HPC UND EXASCALE

# Still An Insatiable Need For Computing

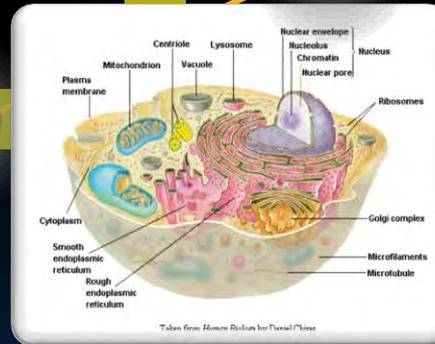
- 1 ZFlops
- 100 EFlops
- 10 EFlops
- 1 EFlops
- 100 PFlops
- 10 PFlops
- 1 PFlops
- 100 TFlops
- 10 TFlops
- 1 TFlops
- 100 GFlops
- 10 GFlops
- 1 GFlops
- 100 MFlops

1993      1999      2005      2011      2017      2023      2029

## Medical Imaging



## Genomics Research



## Weather Prediction



*Forecast*



# The Challenge to Exascale Systems Starts with Power

Operation	Approx Energy Today
Instruction Execution	5-10 pJ
FP operation	200 pJ
Byte read from cache	10-20 pJ
Byte read from DRAM	1.5 nJ
Byte over IC fabric	5 pJ/hop—250 pJ+

9.89MW

8.773PF

1.1GW

151MW\*

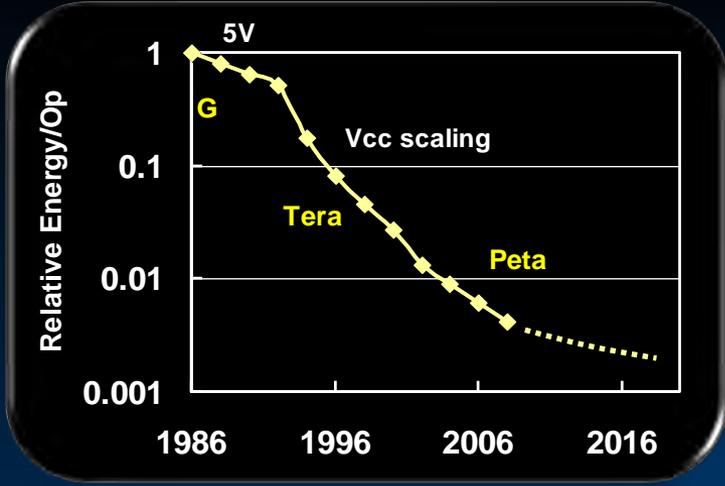
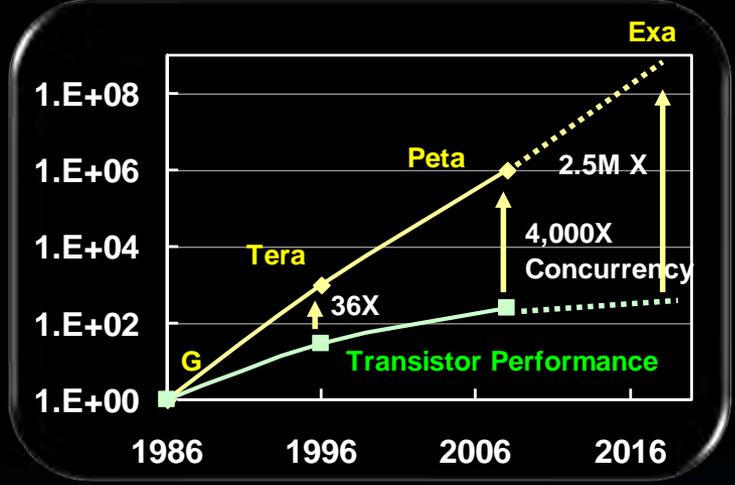
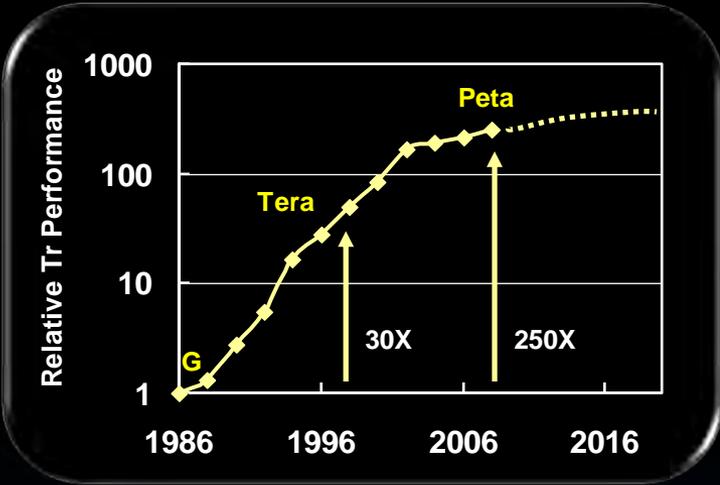
\$1M

\* Assuming 18% Power/Perf CAGR

Source: <http://www.top500.org/lists/2011/06>



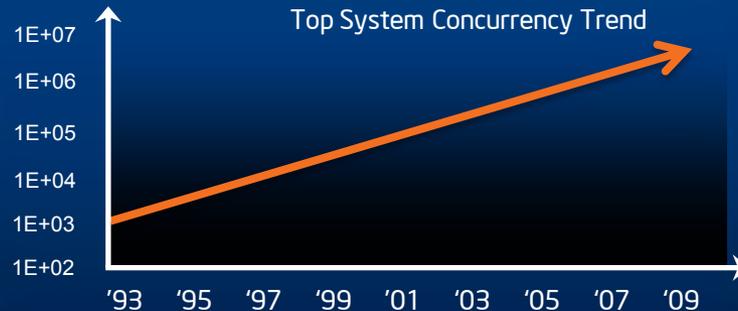
# Technologies and Solutions That Got Us to Petascale...



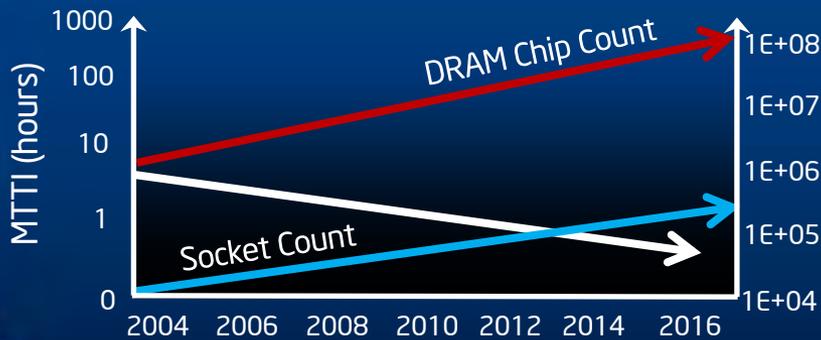
...Will Not Get Us To Exascale 

# The Reliability and Concurrency Challenge to Exascale

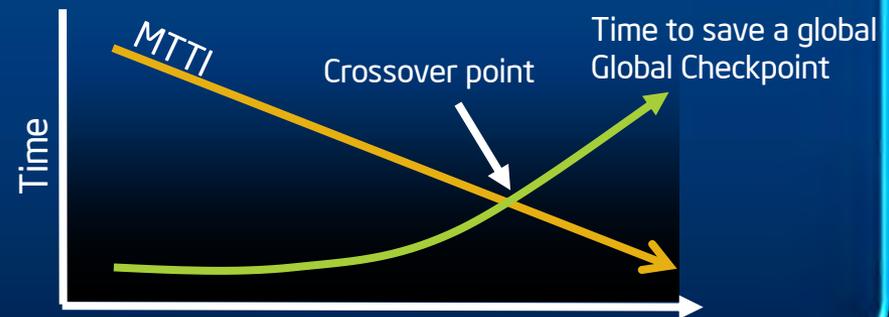
## Extreme Parallelism



## MTTI Measured in Minutes



0.1 Failures per socket per year:



# A Paradigm Shift Is Needed

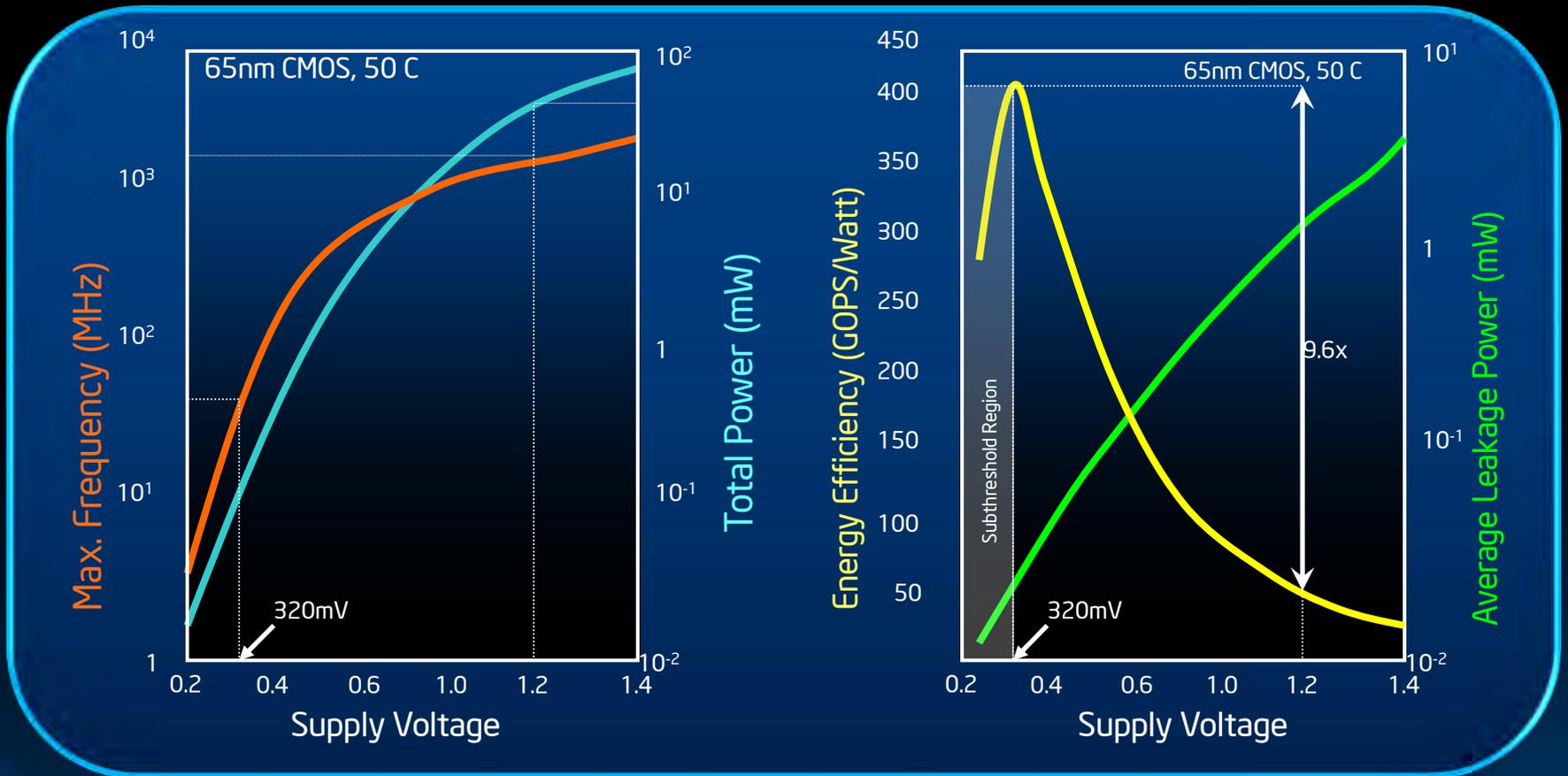
## Past Priorities

Single thread performance	Through Frequency
Programming productivity	Architecture features for productivity
Constraints	(1) Cost (2) Reasonable Power/Energy

## Future Priorities

Throughput performance	Parallelism
Power/Energy	Architecture features for energy Simplicity
Constraints	(1) Programming productivity (2) Cost/Reliability

# Extreme Voltage Scaling



# Re-think System Level Memory Architecture

Emerging  
memory  
technologies

New levels  
of memory  
hierarchy

Minimize  
data  
movement  
across  
hierarchy

Innovative  
packaging  
and IO  
solutions

# Dealing with Parallelism and Locality Challenges

## Programming

Today's Mindset Needs to Change

## Software

Limitations With the Entire SW Stack

## Architecture

Better Mapping of Code onto Architecture



# Intel European Exascale Labs

**Strong Commitment To Advance Computing Leading Edge:**  
*Intel collaborating with HPC community & European researchers*  
*4 labs in Europe - Exascale computing is the central topic*

ExaScale Computing  
Research Lab, Paris



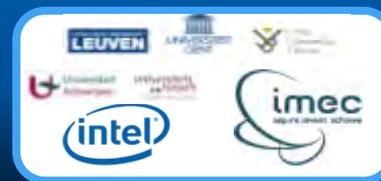
Performance and scalability of  
Exascale applications  
Tools for performance  
characterization

ExaCluster Lab,  
Jülich



Exascale cluster scalability  
and reliability

ExaScience Lab,  
Leuven



Space weather prediction  
Architectural simulation  
Scalable kernels and RT

Intel and BSC Exascale  
Lab, Barcelona



Scalable RTS and tools  
New algorithms

<http://www.exascale-labs.eu>



# Intel European Exascale Labs

## Role

- Understand requirements for Exascale apps
- Provide feedback to Intel HW architects
- Provide guidance to application developers
- Build Exascale HW and SW prototypes
- Contribute to European and national projects

## Status

- Started 2010/2011 as co-design centers
- With leading European HPC R&D organizations
- In total ~70 researchers
- Joint R&D program with partners
- Part of Intel Labs Europe network with >1,500 R&D professionals

# Jülich ExaCluster Laboratory

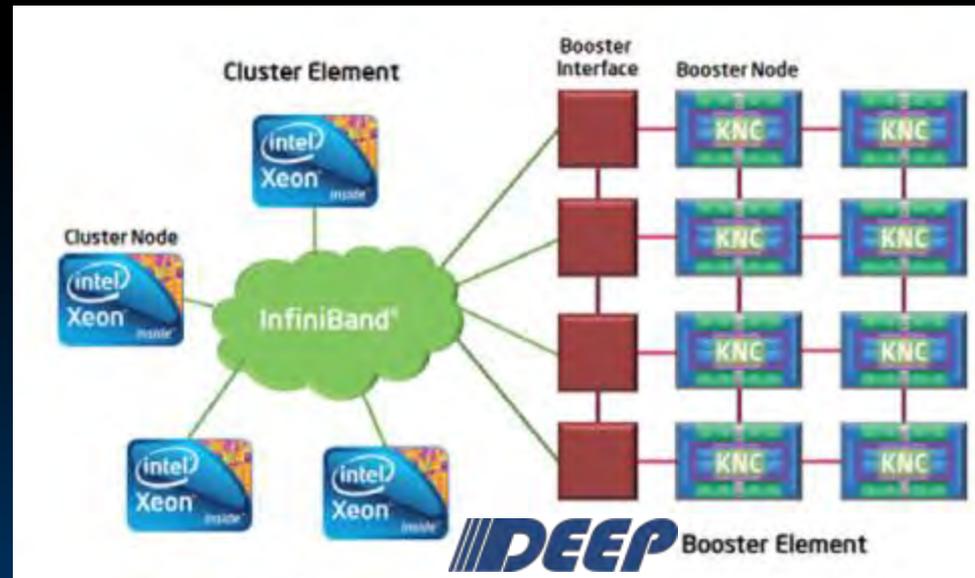


SW Scalability and Resilience

Exascale Cluster Architecture

Exascale Simulation and Tools

## The DEEP Architecture



# Belgium: Flanders ExaScience Lab



Katholieke Universiteit Leuven  
Universiteit Gent  
Vrije Universiteit Brussel  
Universiteit Antwerpen  
Universiteit Hasselt



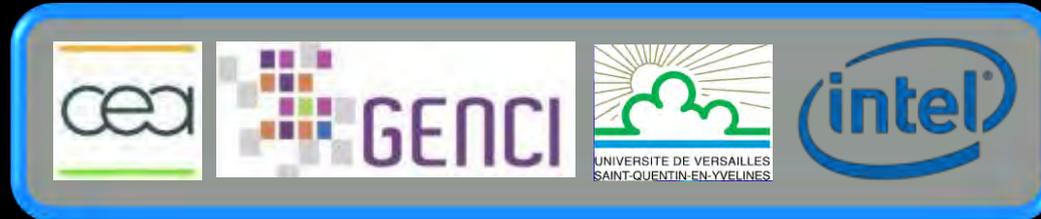
Application  
Frameworks

Exascale  
Space-Weather  
Prediction

Visualization  
Methodologies

Architectural Simulations

# France: Exascale Computing Research Center



Application Scalability

Application Performance  
Characterization/Optimization  
- from Core to Platform level

Geoscience, Life sciences, Energy/Environment

# Barcelona: Intel and BSC Exascale Lab



**Barcelona Supercomputing Center**  
Centro Nacional de Supercomputación



Scalable Performance tools

Scalable Run-time System

New Algorithms

